LF155/LF156/LF355/LF356/LF357
JFET Input Operational Amplifiers

General Description

These are the first monolithic JFET input operational amplifiers to incorporate well matched, high voltage JFETs on the same chip with standard bipolar transistors (BI-FET™ Technology). These amplifiers feature low input bias and offset currents/low offset voltage and offset voltage drift, coupled with offset adjust which does not degrade drift or common-mode rejection. The devices are also designed for high slew rate, wide bandwidth, extremely fast settling time, low voltage and current noise and a low 1/f noise corner.

Advantages

- Replace expensive hybrid and module FET op amps
- Rugged JFETs allow blow-out free handling compared with MOSFET input devices
- Excellent for low noise applications using either high or low source impedance—very low 1/f corner
- Offset adjust does not degrade drift or common-mode rejection as in most monolithic amplifiers
- New output stage allows use of large capacitive loads (5,000 pF) without stability problems
- Internal compensation and large differential input voltage capability

Applications

- Precision high speed integrators
- Fast D/A and A/D converters
- High impedance buffers
- Wideband, low noise, low drift amplifiers
- Logarithmic amplifiers
- Photocell amplifiers
- Sample and Hold circuits

Common Features

- Low input bias current
- Low Input Offset Current
- High input impedance
- Low input noise current
- High common-mode rejection ratio
- Large dc voltage gain

Uncommon Features

- Extremely fast settling time to 0.01%
- Fast slew rate
- Wide gain bandwidth
• Low input noise voltage

Simplified Schematic

Absolute Maximum Ratings (Note 1)

<table>
<thead>
<tr>
<th></th>
<th>LF155/6</th>
<th>LF356B</th>
<th>LF355/6/7</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>±22V</td>
<td>±22V</td>
<td>±18V</td>
</tr>
<tr>
<td>Differential Input Voltage</td>
<td>±40V</td>
<td>±40V</td>
<td>±30V</td>
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<tr>
<td>Input Voltage Range (Note 2)</td>
<td>±120V</td>
<td>±120V</td>
<td>±16V</td>
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<tr>
<td>Output Short Circuit Duration</td>
<td>Continuous</td>
<td>Continuous</td>
<td>Continuous</td>
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<td>$T_{\text{MAX}}$</td>
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<td></td>
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<tr>
<td>H-Package</td>
<td>150°C</td>
<td>115°C</td>
<td>115°C</td>
</tr>
<tr>
<td>N-Package</td>
<td>100°C</td>
<td>100°C</td>
<td>100°C</td>
</tr>
<tr>
<td>M-Package</td>
<td>100°C</td>
<td>100°C</td>
<td>100°C</td>
</tr>
<tr>
<td>Power Dissipation at $T_A = 25{\degree}C$ (Notes 1, δ)</td>
<td></td>
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<tr>
<td>H-Package (Still Air)</td>
<td>560 mW</td>
<td>400 mW</td>
<td>400 mW</td>
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<tr>
<td>H-Package (400 LF/Mn Air Flow)</td>
<td>1200 mW</td>
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<td>1000 mW</td>
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<tr>
<td>N-Package</td>
<td>670 mW</td>
<td>670 mW</td>
<td>670 mW</td>
</tr>
<tr>
<td>M-Package</td>
<td>380 mW</td>
<td>380 mW</td>
<td>380 mW</td>
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<tr>
<td>Thermal Resistance (Typical) $\theta_{IA}$</td>
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</tr>
<tr>
<td>H-Package (Still Air)</td>
<td>160°C/W</td>
<td>160°C/W</td>
<td>160°C/W</td>
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<tr>
<td>H-Package (400 LF/Mn Air Flow)</td>
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<td>65°C/W</td>
<td>65°C/W</td>
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<tr>
<td>N-Package</td>
<td>130°C/W</td>
<td>130°C/W</td>
<td>130°C/W</td>
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<tr>
<td>M-Package</td>
<td>195°C/W</td>
<td>195°C/W</td>
<td>195°C/W</td>
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<tr>
<td>(Typical) $\theta_{JC}$</td>
<td></td>
<td></td>
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<tr>
<td>H-Package</td>
<td>23°C/W</td>
<td>23°C/W</td>
<td>23°C/W</td>
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<td>Storage Temperature Range</td>
<td>-65°C to +150°C</td>
<td>-65°C to +150°C</td>
<td>-65°C to +150°C</td>
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<td>Soldering Information (Lead Temp.)</td>
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<td>Metal Can Package</td>
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<td>Soldering (10 sec.)</td>
<td>300°C</td>
<td>300°C</td>
<td>300°C</td>
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<td>Dual-In-Line Package</td>
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<td>Soldering (10 sec.)</td>
<td>260°C</td>
<td>260°C</td>
<td>260°C</td>
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<tr>
<td>Small Outline Package</td>
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<tr>
<td>Vapor Phase (60 sec.)</td>
<td>215°C</td>
<td>215°C</td>
<td>215°C</td>
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<tr>
<td>Infrared (1s sec.)</td>
<td>220°C</td>
<td>220°C</td>
<td>220°C</td>
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<tr>
<td>ESD tolerance</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>(100 pF discharged through 1.5 kΩ)</td>
<td>1000V</td>
<td>1000V</td>
<td>1000V</td>
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</table>

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.
## DC Electrical Characteristics (Note 3)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>LF155/6</th>
<th>LF356B</th>
<th>LF355/87</th>
<th>Units</th>
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<tbody>
<tr>
<td>( V_{\text{os}} )</td>
<td>Input Offset Voltage</td>
<td>( R_{\text{V}} = 50 \Omega, T_{\text{j}} = 25^\circ \text{C} ) Over Temperature</td>
<td>3</td>
<td>5</td>
<td>3</td>
<td>6.5</td>
</tr>
<tr>
<td>( AV_{\text{op/AT}} )</td>
<td>Average TC of Input Offset Voltage</td>
<td>( R_{\text{V}} = 500 )</td>
<td>5</td>
<td>5</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>( ATC/AV_{\text{op}} )</td>
<td>Change in Average TC with ( V_{\text{op}} ) Adjust</td>
<td>( R_{\text{V}} = 500 ), (Note 4)</td>
<td>0.5</td>
<td>0.5</td>
<td>0.5</td>
<td>( \mu \text{V/}^\circ \text{C} ) per mV</td>
</tr>
<tr>
<td>( I_{\text{os}} )</td>
<td>Input Offset Current</td>
<td>( T_{\text{j}} = 25^\circ \text{C}, ) (Notes 3, 5) ( T_{\text{p}} \leq 7 \text{P}_{\text{in}} )</td>
<td>3</td>
<td>29</td>
<td>3</td>
<td>20</td>
</tr>
<tr>
<td>( I_{\text{in}} )</td>
<td>Input Bias Current</td>
<td>( T_{\text{j}} = 25^\circ \text{C}, ) (Notes 3, 5) ( T_{\text{i}} \leq 7 \text{P}_{\text{in}} )</td>
<td>30</td>
<td>100</td>
<td>30</td>
<td>100</td>
</tr>
<tr>
<td>( R_{\text{in}} )</td>
<td>Input Resistance</td>
<td>( T_{\text{j}} = 25^\circ \text{C} )</td>
<td>10^12</td>
<td>10^12</td>
<td>10^12</td>
<td>( \Omega )</td>
</tr>
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</table>

### Large Signal Voltage Gain
\[ V_{\text{g}} = \pm 1.5 \text{V}, T_{\text{j}} = 25^\circ \text{C} \]
\[ V_{\text{g}} = \pm 10 \text{V}, R_{\text{g}} = 2k \]
Over Temperature
<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>LF153/6</th>
<th>LF355</th>
<th>LF355/87</th>
<th>Units</th>
</tr>
</thead>
</table>
| \( A_{\text{v}} \) | Large Signal Voltage Gain | \( V_{\text{g}} = \pm 1.5 \text{V}, T_{\text{j}} = 25^\circ \text{C} \) \( V_{\text{g}} = \pm 10 \text{V}, R_{\text{g}} = 2k \)
Over Temperature | 50 | 200 | 50 | 200 | 25 | 200 | \( \text{V/mV} \) |

### Output Voltage Swing
\[ V_{\text{g}} = \pm 1.5 \text{V}, R_{\text{g}} = 10k \]
\[ V_{\text{g}} = \pm 10 \text{V}, R_{\text{g}} = 2k \]
Over Temperature
<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>LF153/6</th>
<th>LF355</th>
<th>LF355/87</th>
<th>Units</th>
</tr>
</thead>
</table>
| \( V_{\text{o}} \) | Output Voltage Swing | \( V_{\text{g}} = \pm 1.5 \text{V}, R_{\text{g}} = 10k \) \( V_{\text{g}} = \pm 10 \text{V}, R_{\text{g}} = 2k \)
Over Temperature | ±13 | ±13 | ±12 | ±12 | ±12 | ±12 | ±12 | ±12 | \( \text{V} \) |

### Input Common-Mode Voltage Range
\[ V_{\text{g}} = \pm 1.5 \text{V} \]
<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>LF153/6</th>
<th>LF355</th>
<th>LF355/87</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{\text{cm}} )</td>
<td>Input Common-Mode Voltage Range</td>
<td>( V_{\text{g}} = \pm 1.5 \text{V} )</td>
<td>±11</td>
<td>-12</td>
<td>±11</td>
<td>-12</td>
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### Common-Mode Rejection Ratio (CMRR)
<table>
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<th>LF355/87</th>
<th>Units</th>
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<tr>
<td>CMRR</td>
<td>Common-Mode Rejection Ratio</td>
<td>(Note 6)</td>
<td>85</td>
<td>100</td>
<td>85</td>
<td>100</td>
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### Supply Voltage Rejection Ratio (PSRR)
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<th>LF355</th>
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<th>Units</th>
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<tr>
<td>PSRR</td>
<td>Supply Voltage Rejection Ratio</td>
<td>(Note 6)</td>
<td>85</td>
<td>100</td>
<td>85</td>
<td>100</td>
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### AC Electrical Characteristics

\[ T_{\text{j}} = 25^\circ \text{C}, V_{\text{g}} = \pm 15 \text{V} \]

<table>
<thead>
<tr>
<th>Parameter</th>
<th>LF153</th>
<th>LF355</th>
<th>LF155/355B</th>
<th>LF356</th>
<th>LF357</th>
<th>Units</th>
</tr>
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<tbody>
<tr>
<td>Typ</td>
<td>Max</td>
<td>Typ</td>
<td>Max</td>
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### Slew Rate (SR)
<table>
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<tr>
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<th>Conditions</th>
<th>LF155/355B</th>
<th>LF355</th>
<th>LF355/87</th>
<th>Units</th>
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<tbody>
<tr>
<td>( S_{\text{R}} )</td>
<td>Slew Rate</td>
<td>LF155/8: ( A_{\text{r}} = 1 ), LF355: ( A_{\text{r}} = 5 )</td>
<td>5</td>
<td>7.5</td>
<td>12</td>
<td>50</td>
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### Gain Bandwidth Product (GBW)
<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>LF153/355</th>
<th>LF155/355B</th>
<th>LF355/87</th>
<th>Units</th>
</tr>
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<tbody>
<tr>
<td>Typ</td>
<td>Min</td>
<td>Typ</td>
<td>Typ</td>
<td>Typ</td>
<td>Typ</td>
<td></td>
</tr>
<tr>
<td>GBW</td>
<td>Gain Bandwidth Product</td>
<td>( f = 100 \text{Hz} )</td>
<td>2.5</td>
<td>5</td>
<td>20</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td>( f = 1000 \text{Hz} )</td>
<td>25</td>
<td>15</td>
<td>15</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>( f = 10000 \text{Hz} )</td>
<td>20</td>
<td>12</td>
<td>12</td>
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</table>

### Settling Time (\( t_{\text{S}} \))
<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>LF153/355</th>
<th>LF155/355B</th>
<th>LF355/87</th>
<th>Units</th>
</tr>
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<tbody>
<tr>
<td>Typ</td>
<td>Min</td>
<td>Typ</td>
<td>Typ</td>
<td>Typ</td>
<td>Typ</td>
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<tr>
<td>( t_{\text{S}} )</td>
<td>Settling Time to 0.01%</td>
<td>(Note 7)</td>
<td>4</td>
<td>1.5</td>
<td>1.5</td>
<td>μs</td>
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### Equivalent Input Noise Voltage (\( e_{\text{in}} \))
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<th>Conditions</th>
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<th>LF155/355B</th>
<th>LF355/87</th>
<th>Units</th>
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<tbody>
<tr>
<td>Typ</td>
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<td>Typ</td>
<td>Typ</td>
<td>Typ</td>
<td>Typ</td>
<td></td>
</tr>
<tr>
<td>( e_{\text{in}} )</td>
<td>Equivalent Input Noise Voltage</td>
<td>( R_{\text{g}} = 100 \text{kΩ} ) ( f = 100 \text{Hz} )</td>
<td>25</td>
<td>15</td>
<td>15</td>
<td>V/√Hz</td>
</tr>
<tr>
<td></td>
<td>( f = 1000 \text{Hz} )</td>
<td>20</td>
<td>12</td>
<td>12</td>
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### Equivalent Input Current Noise (\( I_{\text{in}} \))
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<th>LF155/355B</th>
<th>LF355/87</th>
<th>Units</th>
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<tbody>
<tr>
<td>Typ</td>
<td>Min</td>
<td>Typ</td>
<td>Typ</td>
<td>Typ</td>
<td>Typ</td>
<td></td>
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<tr>
<td>( I_{\text{in}} )</td>
<td>Equivalent Input Current Noise</td>
<td>( f = 100 \text{Hz} )</td>
<td>0.01</td>
<td>0.01</td>
<td>0.01</td>
<td>V/√Hz</td>
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<tr>
<td></td>
<td>( f = 1000 \text{Hz} )</td>
<td>0.01</td>
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### Input Capacitance (\( C_{\text{in}} \))
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<th>LF155/355B</th>
<th>LF355/87</th>
<th>Units</th>
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<tr>
<td>Typ</td>
<td>Min</td>
<td>Typ</td>
<td>Typ</td>
<td>Typ</td>
<td>Typ</td>
<td></td>
</tr>
<tr>
<td>( C_{\text{in}} )</td>
<td>Input Capacitance</td>
<td></td>
<td>3</td>
<td>3</td>
<td>3</td>
<td>pF</td>
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</tbody>
</table>
Notes for Electrical Characteristics

Note 1: The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by TJMAX, JA, and the ambient temperature, TA. The maximum available power dissipation at any temperature is 
Pd=(TJMAX-TA)/JA or the 25°C PdMAX, whichever is less.

Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 3: Unless otherwise stated, these test conditions apply:

and VOS, IB and IOS are measured at VCM=0.

Note 4: The Temperature Coefficient of the adjusted input offset voltage changes only a small amount (0.5µV/°C typically) for each mV of adjustment from its original unadjusted value. Common-mode rejection and open loop voltage gain are also unaffected by offset adjustment.

Note 5: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, TJ. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, Pd. TJ=TA+JA Pd where JA is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

Note 6: Supply Voltage Rejection is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

Note 7: Settling time is defined here, for a unity gain inverter connection using 2 kΩ resistors for the LF155/6. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10V step input is applied to the inverter. For the LF357, AV=-5, the feedback resistor from output to input is 2 kΩ and the output step is 10V (See Settling Time Test Circuit).

Note 8: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

Typical DC Performance Characteristics

Curves are for LF155 and LF156 unless otherwise specified.
Typical AC Performance Characteristics

Gain Bandwidth

Normalized Slow Rate

Output Impedance
Detailed Schematic

Connection Diagrams (Top Views)

Application Hints

These are op amps with JFET input devices. These JFETs have large reverse breakdown
voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit. Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode. Exceeding the positive common-mode limit on a single input will not change the phase of the output however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state. These amplifiers will operate with the common-mode input voltage equal to the positive supply. In fact, the common-mode voltage can exceed the positive supply by approximately 100 mV independent of supply voltage and over the full operating temperature range. The positive supply can therefore be used as a reference on an input as, for example, in a supply current monitor and/or limiter.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit. All of the bias currents in these amplifiers are set by FET current sources. The drain currents for the amplifiers are therefore essentially independent of supply voltage. As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize “pickup” and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to ac ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

**Typical Circuit Connections**

![Typical Circuit Connections](image-url)
- VOS is adjusted with a 25k potentiometer
- The potentiometer wiper is connected to V+
- For potentiometers with temperature coefficient of 100 ppm/°C or less the additional drift with adjust is 0.5 µV/°C/mV of adjustment
- Typical overall drift: 5 µV/°C ±(0.5 µV/°C/mV of adj.)

* LF155/6 R = 5k
LF357 R=1.25k
Due to a unique output stage design, these amplifiers have the ability to drive large capacitive loads and still maintain stability.
CL(MAX) = 0.01 µF.
Overshoot ≤ 20%
Settling time (ts) ≅ 5 µs

For distortion ≤ 1% and a 20 Vp-p VOUT swing, power bandwidth is: 500 kHz.
Typical Applications

- Settling time is tested with the LF155/6 connected as unity gain inverter and LF357 connected for AV = -5
- FET used to isolate the probe capacitance
- Output = 10V step
- AV = -5 for LF357
• $\Delta V_{OUT}/\Delta T = \pm 0.002\%/^\circ C$
• All resistors and potentiometers should be wire-wound
• P1: drift adjust
• P2: $V_{OUT}$ adjust
• Use LF155 for
  - Low IB
  - Low drift
  - Low supply current

**Fast Logarithmic Converter**

- Dynamic range: $100 \mu A \leq I_i \leq 1 mA$ (5 decades), $|V_O| = 1 V$/decade
- Transient response: $3 \mu s$ for $\Delta I_i = 1$ decade
- C1, C2, R2, R3: added dynamic compensation
- VOS adjust the LF156 to minimize quiescent error
- RT: Tel Labs type Q81 + 0.3%/°C
\[
\left|\frac{V_{\text{OUT}}}{I_{\text{IN}}\text{m}}\right| = \frac{\left(1 + \frac{R_2}{R_1}\right) \ln\left(\frac{R_T}{R_{\text{REF}}}\right)}{q} \ln \left(\frac{R_T}{R_{\text{REF}}}\right)
\]

**Precision Current Monitor**

- VO=5 R1/R2 (V/mA of IS)
- R1, R2, R3: 0.1% resistors
- Use LF155 for
  - Common-mode range to supply range
  - Low IB
  - Low VOS
  - Low Supply Current

---

**8-Bit D/A Converter with Symmetrical Offset Binary Operation**

- R1, R2 should be matched within ±0.05%
- Full-scale response time: 3 µs

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<thead>
<tr>
<th>Eo</th>
<th>B1</th>
<th>B2</th>
<th>B3</th>
<th>B4</th>
<th>B5</th>
<th>B6</th>
<th>B7</th>
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<td>Negative Full-Scale</td>
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</table>

**Wide BW Low Noise, Low Drift Amplifier**
• Power BW: \( f_{\text{MAX}} = \frac{5}{2nV_p} \approx 191 \text{ kHz} \)

• Parasitic input capacitance \( C_1 \approx (3 \text{ pF for LF155, LF156 and LF357 plus any additional layout capacitance}) \) interacts with feedback elements and creates undesirable high frequency pole. To compensate add \( C_2 \) such that: \( R_2 C_2 \approx R_1 C_1 \).

Boosting the LF156 with a Current Amplifier

- \( \text{OUT(MAX)} \approx 150 \text{ mA (will drive RL} \geq 100 \Omega) \)
- No additional phase shift added by the current amplifier

\[-\frac{\Delta V_{\text{OUT}}}{\Delta T} = \frac{0.15}{10^{-2}} \text{ V/} \mu\text{s (with } C_L \text{ shown)}\]

3 Decades VCO
Overshoot 6%

- ts 10 µs

When driving large CL, the VOUT slew rate determined by CL and IOUT(MAX):

\[ \frac{\Delta V_{\text{OUT}}}{\Delta t} = \frac{I_{\text{OUT}}}{C_L} \approx \frac{0.2}{0.5} \text{V/µs} = 0.34 \text{V/µs (with } C_L \text{ shown)} \]

- By adding D1 and Rf, VD1=0 during hold mode. Leakage of D2 provided by feedback path through Rf.
- Leakage of circuit is essentially Ib (LF155, LF156) plus capacitor leakage of Cp.
- Diode D3 clamps VOUT (A1) to VIN-VD3 to improve speed and to limit reverse bias of D2.
- Maximum input frequency should be \( << \frac{\pi R_f C_D}{2} \) where \( C_D \) is the shunt capacitance of D2.
Non-Inverting Unity Gain Operation for LF157

$$R_1 C \geq \frac{1}{(2\pi)(5 \text{ MHz})}$$

$$R_1 = \frac{R_2 + R_0}{4}$$

$$A_V(\text{DC}) = 1$$

$$f_{-3dB} \approx 5 \text{ MHz}$$

Inverting Unity Gain for LF157

$$R_1 C \geq \frac{1}{(2\pi)(5 \text{ MHz})}$$

$$R_1 = \frac{R_2}{4}$$

$$A_V(\text{DC}) = -1$$

$$f_{-3dB} \approx 5 \text{ MHz}$$

High Impedance, Low Drift Instrumentation Amplifier
- $V_{\text{OUT}} = \frac{R_3}{R} \left[ \frac{2R \Delta V}{R_1} + 1 \right]$ $\Delta V, \sqrt{V^2 + 2V} \leq V_{\text{IN}} \text{ common-mode} \leq V^+$

- System VOS adjusted via A2 VOS adjust
- Trim R3 to boost up CMRR to 120 dB. Instrumentation amplifier resistor array recommended for best accuracy and lowest drift

Both amplifiers (A1, A2) have feedback loops individually closed with stable responses (overshoot negligible)
- Acquisition time $T_A$, estimated by:

$$T_A \approx \left[ \frac{2R_{\text{ON}} V_{\text{IN}} C_{\text{th}}}{1 + 2} \right]^{1/2}$$ provided that:

$$V_{\text{IN}} < 2\pi \tau R_{\text{ON}} C_{\text{th}} \text{ and } T_A > \frac{V_{\text{IN}} C_{\text{th}}}{1 + 2}$$ $R_{\text{ON}}$ of SW1

If inequality not satisfied: $T_A \approx \frac{V_{\text{IN}} C_{\text{th}}}{2 \pi \tau}$

- LF156 develops full Sr output capability for $V_{\text{IN}} \geq 1V$
- Addition of SW2 improves accuracy by putting the voltage drop across SW1 inside the feedback loop
- Overall accuracy of system determined by the accuracy of both amplifiers, A1 and A2
By closing the loop through A2, the VOUT accuracy will be determined uniquely by A1. No VOS adjust required for A2.

TA can be estimated by same considerations as previously but, because of the added propagation delay in the feedback loop (A2) the overshoot is not negligible.

Overall system slower than fast sample and hold

R1, CC: additional compensation

Use LF156 for
- Fast settling time
- Low VOS

By adding positive feedback (R2)

Q increases to 40

fBP=100 kHz
\[
\frac{V_{OUT}}{V_{IN}} = 10 \sqrt{Q}
\]

- Clean layout recommended
- Response to a 1 Vp-p tone burst: 300 µs

![High Q Notch Filter](image)

- \(2R1 = R = 10 \, \text{M\Omega}\)
- \(2C = C1 = 300 \, \text{pF}\)
- Capacitors should be matched to obtain high Q
- \(f\text{NOTCH} = 120 \, \text{Hz}, \text{notch} = -55 \, \text{dB}, Q > 100\)
- Use LF155 for
  - Low IB
  - Low supply current
OPA111

Low Noise Precision Difet®
OPERATIONAL AMPLIFIER

FEATURES

- LOW NOISE: 100% Tested, 8nV/√Hz max (10kHz)
- LOW BIAS CURRENT: 1pA max
- LOW OFFSET: 250µV max
- LOW DRIFT: 1µV/°C max
- HIGH OPEN-LOOP GAIN: 120dB min
- HIGH COMMON-MODE REJECTION: 100dB min

DESCRIPTION

The OPA111 is a precision monolithic dielectrically isolated FET (Difet®) operational amplifier. Outstanding performance characteristics allow its use in the most critical instrumentation applications. Noise, bias current, voltage offset, drift, open-loop gain, common-mode rejection, and power supply rejection are superior to BIFET® amplifiers. Very low bias current is obtained by dielectric isolation with on-chip guarding. Laser trimming of thin-film resistors gives very low offset and drift. Extremely low noise is achieved with patented circuit design techniques. A new cascode design allows high precision input specifications and reduced susceptibility to flicker noise. Standard 741 pin configuration allows upgrading of existing designs to higher performance levels.

APPLICATIONS

- PRECISION INSTRUMENTATION
- DATA ACQUISITION
- TEST EQUIPMENT
- OPTOELECTRONICS
- MEDICAL EQUIPMENT—CAT SCANNER
- RADIATION HARD EQUIPMENT
# SPECIFICATIONS

## ELECTRICAL

At VCC = ±15VDC and TA = +25°C unless otherwise noted.

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<thead>
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<th>CONDITION</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
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<th>TYP</th>
<th>MAX</th>
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<td>±s</td>
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<td>±V</td>
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<td>Biases</td>
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<td>-25</td>
<td>±5</td>
<td>-25</td>
<td>±5</td>
<td>-25</td>
<td>±5</td>
<td>±V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Φ: Junction-Ambient</td>
<td></td>
<td>200</td>
<td>±15</td>
<td>200</td>
<td>±15</td>
<td>200</td>
<td>±15</td>
<td>±℃</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**NOTES:**
1. Sample tested—this parameter is guaranteed.
2. Offset voltage, offset current, and bias current are measured with the units fully warmed up.
3. Overload recovery is defined as the time required for the output to return from saturation to linear operation following the removal of a 50% input overdrive.
### ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

At $VCC = \pm 15VDC$ and $TA = TMIN$ to $TMAX$ unless otherwise noted.

#### TEMPERATURE RANGE

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>Units</th>
</tr>
</thead>
</table>

#### INPUT

| Offset Voltage Input Offset Voltage Average Drift | $V_{IN} = \pm 1VDC$ | $\pm 50$ | $\pm 25$ | $\pm 12$ | $\pm 6$ | $\pm 3$ | $\pm 1.5$ | $\pm 1.2$ | $\pm 0.3$ | $\pm 0.15$ | $\mu V$ |
| Offset Current Input Offset Current | $V_{IN} = \pm 1VDC$ | $\pm 50$ | $\pm 25$ | $\pm 12$ | $\pm 6$ | $\pm 3$ | $\pm 1.5$ | $\pm 1.2$ | $\pm 0.3$ | $\pm 0.15$ | $pA$ |

#### OUTPUT

| Common-Mode Input Common-Mode Drift | $V_{CM} = \pm 5VDC$ | $\pm 10$ | $\pm 5$ | $\pm 2.5$ | $\pm 1.25$ | $\pm 0.625$ | $\pm 0.3125$ | $\pm 0.15625$ | $\pm 0.078125$ | $\pm 0.0390625$ | $V$ |

#### OPEN-LOOP GAIN, DC

| Open-Loop Gain | $R_L = 2k\Omega$ | $110$ | $120$ | $110$ | $120$ | $110$ | $120$ | $110$ | $120$ | $110$ | $120$ | $%$ |

#### VOLTAGE OUTPUT

| Voltage Output Current Output Short-Circuit Current | $R_L = 2k\Omega$ | $2.5$ | $2.5$ | $2.5$ | $2.5$ | $2.5$ | $2.5$ | $2.5$ | $2.5$ | $2.5$ | $mA$ |

#### POWER SUPPLY

| Current Quiescent | $I_{Q} = 6mA$ | $5$ | $5$ | $5$ | $5$ | $5$ | $5$ | $5$ | $5$ | $5$ | $mA$ |

**NOTES:** (1) Offset voltage, offset current, and bias current are measured with the units fully warmed up.

### CONNECTION DIAGRAM

![Connection Diagram](image)

### ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Supply Voltage</th>
<th>$\pm 20VDC$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Internal Power Dissipation</td>
<td>$\leq 750mW$</td>
</tr>
<tr>
<td>Absolute Input Voltage</td>
<td>$\leq 5VDC$</td>
</tr>
<tr>
<td>Absolute Input Voltage Range</td>
<td>$\leq 5VDC$</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>$-65^\circ C \rightarrow +150^\circ C$</td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>$-65^\circ C \rightarrow +150^\circ C$</td>
</tr>
<tr>
<td>Over Temperature (max)</td>
<td>$100^\circ C$</td>
</tr>
<tr>
<td>Output Short Circuit Duration</td>
<td>Continuous</td>
</tr>
<tr>
<td>Junction Temperature</td>
<td>$+175^\circ C$</td>
</tr>
</tbody>
</table>

**NOTES:** (1) Package must be derated below $V_{CC} = \pm 50V$ or $V_{CC} = \pm 30V$.
(2) See supply voltage for $+8V$, the absolute maximum input voltage is equal to $+8V > V_{IN} > -8V$, see Figure 2.
(3) Short circuit may be $0V > V_{OUT} > -V_{CC}$. Rating applies to $0^\circ C$ ambient. Observe discharge limit for $T_{J}$.
PACKAGE INFORMATION

<table>
<thead>
<tr>
<th>MODEL</th>
<th>PACKAGE</th>
<th>PACKAGE DRAWING NUMBER</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPA111AM</td>
<td>TO-93</td>
<td>001</td>
</tr>
<tr>
<td>OPA111BM</td>
<td>TO-93</td>
<td>001</td>
</tr>
<tr>
<td>OPA111SM</td>
<td>TO-93</td>
<td>001</td>
</tr>
</tbody>
</table>

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

<table>
<thead>
<tr>
<th>MODEL</th>
<th>PACKAGE</th>
<th>TEMPERATURE RANGE</th>
<th>OFFSET VOLTAGE, MAX (mV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPA111AM</td>
<td>TO-99</td>
<td>-25°C to +85°C</td>
<td>2500</td>
</tr>
<tr>
<td>OPA111BM</td>
<td>TO-99</td>
<td>-25°C to +85°C</td>
<td>2500</td>
</tr>
<tr>
<td>OPA111SM</td>
<td>TO-99</td>
<td>-25°C to +150°C</td>
<td>2500</td>
</tr>
</tbody>
</table>

DICE INFORMATION

OPA111AD DIE TOPOGRAPHY

MECHANICAL INFORMATION

<table>
<thead>
<tr>
<th>MILL (0.001&quot;)</th>
<th>MILLIMETER</th>
</tr>
</thead>
<tbody>
<tr>
<td>Die Size</td>
<td>2.41 x 1.00 x 2.15</td>
</tr>
<tr>
<td>Min. Pad Size</td>
<td>0.10 x 0.10</td>
</tr>
</tbody>
</table>

Substrate Bias: This Dielectrically-Isolated Substrate is normally connected to common.
TYPICAL PERFORMANCE CURVES

TA = +25°C, VCC = ±15VDC unless otherwise noted.
APPLICATIONS INFORMATION

OFFSET VOLTAGE ADJUSTMENT

The OPA111 offset voltage is laser-trimmed and will require no further trim for most applications. As with most amplifiers, externally trimming the remaining offset can change drift performance by about 0.3µV/°C for each 100µV of adjusted offset. Note that the trim (Figure 1) is similar to operational amplifiers such as 741 and AD547. The OPA111 can replace most other amplifiers by leaving the external null circuit unconnected.

INPUT PROTECTION

Conventional monolithic FET operational amplifiers require external current-limiting resistors to protect their inputs against destructive currents that can flow when input FET gate-to-substrate isolation diodes are forward-biased. Most BIFET amplifiers can be destroyed by the loss of –VCC.
Unlike BIFET amplifiers, The **Difet** OPA111 requires input current limiting resistors only if its input voltage is greater than 6V more negative than –VCC. A 10kΩ series resistor will limit input current to a safe level with up to ±15V input levels, even if both supply voltages are lost.

![Input Current vs Input Voltage with ±VCC Pins Grounded.](image)

Static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers (both bipolar and FET types), this may cause a noticeable degradation of offset voltage and drift. Static protection is recommended when handling any precision IC operational amplifier.

**GUARDING AND SHIELDING**

As in any situation where high impedances are involved, careful shielding is required to reduce “hum” pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry. Leakage currents across printed circuit boards can easily exceed the bias current of the OPA111. To avoid leakage problems, it is recommended that the signal input lead of the OPA111 be wired to a Teflon standoff. If the OPA111 is to be soldered directly into a printed circuit board, utmost care must be used in planning the board layout. A “guard” pattern should completely surround the high impedance input leads and should be connected to a low impedance point which is at the signal input potential. The amplifier case should be connected to any input shield or guard via pin 8. This insures that the amplifier itself is fully surrounded by guard potential, minimizing both leakage and noise pickup (see Figure 3). If guarding is not required, pin 8 (case) should be connected to ground.

![Connection of Input Guard.](image)
NOISE: FET VERSUS BIPOLAR

Low noise circuit design requires careful analysis of all noise sources. External noise sources can dominate in many cases, so consider the effect of source resistance on overall operational amplifier noise performance. At low source impedances, the lower voltage noise of a bipolar operational amplifier is superior, but at higher impedances the high current noise of a bipolar amplifier becomes a serious liability. Above about 15kΩ, the OPA111 will have a lower total noise than an OP-27 (see Figure 4).


BIAS CURRENT CHANGE VERSUS COMMON-MODE VOLTAGE

The input bias current of most popular BIFET operational amplifiers are affected by common-mode voltage (Figure 5). Higher input FET gate-to-drain voltage causes leakage and ionization (bias) currents to increase. Due to its cascode input stage, the extremely low bias current of the OPA111 is not compromised by common-mode voltage.

FIGURE 5. Input Bias Current vs Common-Mode Voltage.

APPLICATIONS CIRCUITS

Figures 6 through 18 are circuit diagrams of various applications for the OPA111.
FIGURE 6. Pyroelectric Infrared Detector.


FIGURE 9. High Impedance (10^14 Ω) Amplifier.


FIGURE 11. 60Hz Reject Filter.
FIGURE 12. Piezoelectric Transducer Charge Amplifier.

FIGURE 13. 0.6Hz Second-Order Low-Pass Filter.

FIGURE 14. RIAA Equalized Phono Preamplifier.

FIGURE 15. High Sensitivity (under 1nW) Fiber Optic Receiver for 9600 Baud Manchester Data.

FIGURE 16. 'N' Stage Parallel-Input Amplifier for Reduced Relative Amplifier Noise at the Output.
FIGURE 17. FET Input Instrumentation Amplifier.

FIGURE 18. Low-Droop Positive Peak Detector.
ICL8038
Precision Waveform Generator/Voltage Controlled Oscillator

Features
- Low Frequency Drift with Temperature ... 250ppm/oC
- Low Distortion .............. 1% (Sine Wave Output)
- High Linearity .......... 0.1% (Triangle Wave Output)
- Wide Frequency Range ......... 0.001Hz to 300kHz
- Variable Duty Cycle ............... 2% to 98%
- High Level Outputs ............... TTL to 28V
- Simultaneous Sine, Square, and Triangle Wave Outputs
- Easy to Use - Just a Handful of External Components Required

Description
The ICL8038 waveform generator is a monolithic integrated circuit capable of producing high accuracy sine, square, triangular, sawtooth and pulse waveforms with a minimum of external components. The frequency (or repetition rate) can be selected externally from 0.001Hz to more than 300kHz using either resistors or capacitors, and frequency modulation and sweeping can be accomplished with an external voltage. The ICL8038 is fabricated with advanced monolithic technology, using Schottky barrier diodes and thin film resistors, and the output is stable over a wide range of temperature and supply variations. These devices may be interfaced with phase locked loop circuitry to reduce temperature drift to less than 250ppm/oC.

Ordering Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>STABILITY</th>
<th>TEMP. RANGE (°C)</th>
<th>PACKAGE</th>
<th>PKS. NO.</th>
</tr>
</thead>
<tbody>
<tr>
<td>ICL8038C01FD</td>
<td>250ppm/°C (Typ)</td>
<td>0 to 70</td>
<td>14 Ld PDIP</td>
<td>F14.3</td>
</tr>
<tr>
<td>ICL8038C01JD</td>
<td>250ppm/°C (Typ)</td>
<td>0 to 70</td>
<td>14 Ld CERDIP</td>
<td>F14.3</td>
</tr>
<tr>
<td>ICL8038C01JD</td>
<td>100ppm/°C (Typ)</td>
<td>0 to 70</td>
<td>14 Ld CERDIP</td>
<td>F14.3</td>
</tr>
<tr>
<td>ICL8038C01JD</td>
<td>120ppm/°C (Typ)</td>
<td>0 to 70</td>
<td>14 Ld CERDIP</td>
<td>F14.3</td>
</tr>
<tr>
<td>ICL8038C01JD (Note)</td>
<td>350ppm/°C (Max)</td>
<td>-55 to 125</td>
<td>14 Ld CERDIP</td>
<td>F14.3</td>
</tr>
<tr>
<td>ICL8038C01JD (Note)</td>
<td>250ppm/°C (Max)</td>
<td>-55 to 125</td>
<td>14 Ld CERDIP</td>
<td>F14.3</td>
</tr>
</tbody>
</table>

NOTE: Add /863D to part number if 865 processing is required.
**Pinout**

ICL8038 (PDIP, CERDIP)

**TOP VIEW**

- Pin 1: SINE WAVE ADJUST
- Pin 2: SINE WAVE OUT
- Pin 3: TRIANGLE OUT
- Pin 4: DUTY CYCLE
- Pin 5: FREQUENCY
- Pin 6: ADJUST
- Pin 7: V-
- Pin 8: FM BIAS
- Pin 9: ¾ OR GND
- Pin 10: TIMING CAPACITOR
- Pin 11: SQUARE WAVE OUT
- Pin 12: FM SINE WAVE OUT
- Pin 13: NC
- Pin 14: NC

**Functional Diagram**

- CURRENT SOURCE #1
- CURRENT SOURCE #2
- COMPARATOR #1
- COMPARATOR #2
- FLIP-FLOP
- BUFFER
- BUFFER
- SIN CONVERTER
- V+
Absolute Maximum Ratings

Supply Voltage (V_+ to V_-) .......................... 36V
Input Voltage (Any Pin) ......................... V_+ to V_-
Input Current (Pins 4 and 5) ...................... 25mA
Output Sink Current (Pins 3 and 9) .............. 25mA

Operating Conditions

Temperature Range
ICL8038AM, ICL8038BM ............................. -55°C to 125°C
ICL8038AC, ICL8038BC, ICL8038CC ............. 0°C to 70°C

Thermal Information

Thermal Resistance (Typical, Note 1)  
  θJA (°C/W)  θJC (°C/W)
CERDIP Package ................................. 75  20
PDIP Package ..................................... 115 N/A
Maximum Junction Temperature (Ceramic Package) ........ 175°C
Maximum Junction Temperature (Plastic Package) ........... 125°C
Maximum Storage Temperature Range ............... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ............ 300°C

NOTE:
1. θJA is measured with the component mounted on an evaluation PC board in free air.
### Electrical Specifications

**VSUPPLY** = ±10V or +20V, TA = ±25°C, RL = 10kΩ, Test Circuit Unless Otherwise Specified

#### NOTES:
1. RA and RB currents not included.
2. VSUPPLY = 20V; RA and RB = 10kΩ, f ≅ 10kHz nominal; can be extended 1000 to 1. See Figures 5A and 5B.
3. 82kΩ connected between pins 11 and 12, Triangle Duty Cycle set at 50%. (Use RA and RB.)
4. Figure 1, pins 7 and 8 connected, VSUPPLY = ±10V. See Typical Curves for T.C. vs VSUPPLY.
5. Not tested, typical value for design purposes only.

#### Supply Voltage Operating Range

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>TEST CONDITIONS</th>
<th>ICL603BC</th>
<th>ICL603BB(EN)</th>
<th>ICL603AC(AM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage Operating Range</td>
<td>VSupply</td>
<td>Single Supply</td>
<td>+10</td>
<td>-</td>
<td>+30</td>
</tr>
<tr>
<td></td>
<td>V+ , V-</td>
<td>Dual Supplies</td>
<td>±5</td>
<td>-</td>
<td>±15</td>
</tr>
</tbody>
</table>

8038AC, 8038CC, 8038CC

<table>
<thead>
<tr>
<th>RA and RB currents not included.</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>TEST CONDITIONS</th>
<th>ICL603BC</th>
<th>ICL603BB(EN)</th>
<th>ICL603AC(AM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency Characteristics</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Max. Frequency of Oscillation</td>
<td>fMAX</td>
<td>100</td>
<td>-</td>
<td>-</td>
<td>100</td>
</tr>
<tr>
<td>Sweep Frequency of FM input</td>
<td>fSWEEP</td>
<td>-</td>
<td>10</td>
<td>-</td>
<td>10</td>
</tr>
<tr>
<td>Sweep FM Range (Note 3)</td>
<td>f ≅ 10kHz</td>
<td>-</td>
<td>35.1</td>
<td>-</td>
<td>35.1</td>
</tr>
<tr>
<td>FM Linearity</td>
<td>0</td>
<td>0.5</td>
<td>-</td>
<td>0.2</td>
<td>-</td>
</tr>
<tr>
<td>Frequency Drift with Temperature (Note 5)</td>
<td>fMAX</td>
<td>0°C to 70°C</td>
<td>-</td>
<td>250</td>
<td>-</td>
</tr>
<tr>
<td>8038AC, 8038CC, 8038CC</td>
<td>-50°C to 125°C</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>350</td>
</tr>
<tr>
<td>Frequency Drift with Supply Voltage</td>
<td>fMAX</td>
<td>Over Supply Voltage Range</td>
<td>-</td>
<td>0.05</td>
<td>-</td>
</tr>
</tbody>
</table>

#### Output Characteristics

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>TEST CONDITIONS</th>
<th>ICL603BC</th>
<th>ICL603BB(EN)</th>
<th>ICL603AC(AM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Impedance</td>
<td>ZOUT</td>
<td>Input = 5mA</td>
<td>-</td>
<td>200</td>
<td>-</td>
</tr>
<tr>
<td>Sine Wave Amplitude</td>
<td>Vsin</td>
<td>Rsine = 10kΩ</td>
<td>0.2</td>
<td>0.23</td>
<td>-</td>
</tr>
<tr>
<td>THD</td>
<td>THD</td>
<td>Rsine = 10kΩ (Note 4)</td>
<td>-</td>
<td>2.0</td>
<td>5</td>
</tr>
</tbody>
</table>

#### Triangle/Sawtooth/Ramp

| Amplitude | Vtriangle | Ptriangle = 100kHz | 0.30 | 0.30 | 0.30 | 0.30 | 0.30 | 0.30 | x VSupply |
| Linearity | - | 0.05 | - | 0.05 | - | 0.05 | - | 0.05 | - | % |

#### NOTES:

2. RA and RB currents not included.
3. VSUPPLY = 20V; RA and RB = 10kΩ, f ≅ 10kHz nominal; can be extended 1000 to 1. See Figures 5A and 5B.
4. 82kΩ connected between pins 11 and 12, Triangle Duty Cycle set at 50%. (Use RA and RB.)
5. Figure 1, pins 7 and 8 connected, VSUPPLY = ±10V. See Typical Curves for T.C. vs VSUPPLY.
6. Not tested, typical value for design purposes only.
Test Conditions

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>$R_A$</th>
<th>$R_B$</th>
<th>$R_L$</th>
<th>$C$</th>
<th>SW</th>
<th>MEASURE</th>
</tr>
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<tbody>
<tr>
<td>Supply Current</td>
<td>10kΩ</td>
<td>10kΩ</td>
<td>10kΩ</td>
<td>3.3μF</td>
<td>Closed</td>
<td>Current into Pin 6</td>
</tr>
<tr>
<td>Sweep FM Range (Note 7)</td>
<td>10kΩ</td>
<td>10kΩ</td>
<td>10kΩ</td>
<td>3.3μF</td>
<td>Open</td>
<td>Frequency at Pin 9</td>
</tr>
<tr>
<td>Frequency Drift with Temperature</td>
<td>10kΩ</td>
<td>10kΩ</td>
<td>10kΩ</td>
<td>3.3μF</td>
<td>Closed</td>
<td>Frequency at Pin 3</td>
</tr>
<tr>
<td>Frequency Drift with Supply Voltage (Note 8)</td>
<td>10kΩ</td>
<td>10kΩ</td>
<td>10kΩ</td>
<td>3.3μF</td>
<td>Closed</td>
<td>Frequency at Pin 9</td>
</tr>
<tr>
<td>Output Amplitude (Note 10)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sine</td>
<td>10kΩ</td>
<td>10kΩ</td>
<td>10kΩ</td>
<td>3.3μF</td>
<td>Closed</td>
<td>Pk-Pk Output at Pin 2</td>
</tr>
<tr>
<td>Triangle</td>
<td>10kΩ</td>
<td>10kΩ</td>
<td>10kΩ</td>
<td>3.3μF</td>
<td>Closed</td>
<td>Pk-Pk Output at Pin 3</td>
</tr>
<tr>
<td>Leakage Current (Off; Note 9)</td>
<td>10kΩ</td>
<td>10kΩ</td>
<td>10kΩ</td>
<td>3.3μF</td>
<td>Closed</td>
<td>Current into Pin 9</td>
</tr>
<tr>
<td>Saturation Voltage (On) (Note 9)</td>
<td>10kΩ</td>
<td>10kΩ</td>
<td>10kΩ</td>
<td>3.3μF</td>
<td>Closed</td>
<td>Output (Low) at Pin 9</td>
</tr>
<tr>
<td>Rise and Fall Times (Note 11)</td>
<td>10kΩ</td>
<td>10kΩ</td>
<td>4.7kΩ</td>
<td>3.3μF</td>
<td>Closed</td>
<td>Waveform at Pin 9</td>
</tr>
<tr>
<td>Duty Cycle Adjust (Note 11)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Max</td>
<td>50kΩ</td>
<td>-1.0kΩ</td>
<td>10kΩ</td>
<td>3.3μF</td>
<td>Closed</td>
<td>Waveform at Pin 9</td>
</tr>
<tr>
<td>Min</td>
<td>-25kΩ</td>
<td>50kΩ</td>
<td>10kΩ</td>
<td>3.3μF</td>
<td>Closed</td>
<td>Waveform at Pin 9</td>
</tr>
<tr>
<td>Triangle Waveform Linearity</td>
<td>10kΩ</td>
<td>10kΩ</td>
<td>10kΩ</td>
<td>3.3μF</td>
<td>Closed</td>
<td>Waveform at Pin 3</td>
</tr>
<tr>
<td>Total Harmonic Distortion</td>
<td>10kΩ</td>
<td>10kΩ</td>
<td>10kΩ</td>
<td>3.3μF</td>
<td>Closed</td>
<td>Waveform at Pin 2</td>
</tr>
</tbody>
</table>

NOTES:
7. The hi and lo frequencies can be obtained by connecting pin 8 to pin 7 (hi) and then connecting pin 8 to pin 6 (lo). Otherwise apply Sweep Voltage at pin 8 (2/3 VSUPPLY +2V) ≤ VSWEEP ≤ VSUPPLY where VSUPPLY is the total supply voltage. In Figure 5B, pin 8 should vary between 5.3V and 10V with respect to ground.
8. 10V ≤ V+ ≤ 30V, or ±5V ≤ VSUPPLY ≤ ±15V.
9. Oscillation can be halted by forcing pin 10 to +5V or -5V.
10. Output Amplitude is tested under static conditions by forcing pin 10 to 5V then to -5V.
11. Not tested; for design purposes only.

Test Circuit

FIGURE 1. TEST CIRCUIT
APPLICATION INFORMATION (See Functional Diagram)

An external capacitor C is charged and discharged by two current sources. Current source #2 is switched on and off by a flip-flop, while current source #1 is on continuously. Assuming that the flip-flop is in a state such that current source #2 is off, and the capacitor is charged with a current I, the voltage across the capacitor rises linearly with time. When this voltage reaches the level of comparator #1 (set at 2/3 of the supply voltage), the flip-flop is triggered, changes states, and releases current source #2. This current source normally carries a current 2I, thus the capacitor is discharged with a net-current I and the voltage across it drops linearly with time. When it has reached the level of comparator #2 (set at 1/3 of the supply voltage), the flip-flop is triggered into its original state and the cycle starts again.

Four waveforms are readily obtainable from this basic generator circuit. With the current sources set at I and 2I respectively, the charge and discharge times are equal. Thus a triangle waveform is created across the capacitor and the flip-flop produces a square wave. Both waveforms are fed to buffer stages and are available at pins 3 and 9.

The levels of the current sources can, however, be selected over a wide range with two external resistors. Therefore, with the two currents set at values different from I and 2I, an asymmetrical sawtooth appears at Terminal 3 and pulses with a duty cycle from less than 1% to greater than 99% are available at Terminal 9.
The sine wave is created by feeding the triangle wave into a nonlinear network (sine converter). This network provides a decreasing shunt impedance as the potential of the triangle moves toward the two extremes.

**Waveform Timing**

The symmetry of all waveforms can be adjusted with the external timing resistors. Two possible ways to accomplish this are shown in Figure 3. Best results are obtained by keeping the timing resistors RA and RB separate (A). RA controls the rising portion of the triangle and sine wave and the 1 state of the square wave. The magnitude of the triangle waveform is set at 1/3 VSUPPLY; therefore the rising portion of the triangle is,

\[ t_1 = \frac{C \times V}{1} - \frac{C \times \frac{1}{3} \times V_{\text{SUPPLY}} \times R_A}{0.22 \times V_{\text{SUPPLY}}} = \frac{R_A \times C}{0.66} \]

The falling portion of the triangle and sine wave and the 0 state of the square wave is:

\[ t_2 = \frac{C \times V}{1} - \frac{C \times \frac{1}{3} V_{\text{SUPPLY}}}{R_B} - \frac{V_{\text{SUPPLY}}}{R_A} = \frac{R_A R_B C}{0.66(2R_A - R_B)} \]

Thus a 50% duty cycle is achieved when RA = RB.

If the duty cycle is to be varied over a small range about 50% only, the connection shown in Figure 3B is slightly more convenient. A 1kΩ potentiometer may not allow the duty cycle to be adjusted through 50% on all devices. If a 50% duty cycle is required, a 2kΩ or 5kΩ potentiometer should be used.

With two separate timing resistors, the frequency is given by:

\[ f = \frac{1}{\pi} \frac{1}{t_1 + t_2} = \frac{1}{\frac{RA \times C}{0.66} + \frac{RB}{0.66(2RA - RB)}} \]

or, if RA = RB = R

\[ f = \frac{0.33}{RC} \] (for Figure 3A)

Neither time nor frequency are dependent on supply voltage, even though none of the voltages are regulated inside the integrated circuit. This is due to the fact that both currents and thresholds are direct, linear functions of the supply voltage and thus their effects cancel.

![FIGURE 2A. SQUARE WAVE DUTY CYCLE - 50%](image1)

![FIGURE 2B. SQUARE WAVE DUTY CYCLE - 80%](image2)

**FIGURE 2. PHASE RELATIONSHIP OF WAVEFORMS**
Reducing Distortion

To minimize sine wave distortion the 82k resistor between pins 11 and 12 is best made variable. With this arrangement distortion of less than 1% is achievable. To reduce this even further, two potentiometers can be connected as shown in Figure 4; this configuration allows a typical reduction of sine wave distortion close to 0.5%.

Selecting RA, RB and C

For any given output frequency, there is a wide range of RC combinations that will work, however certain constraints are placed upon the magnitude of the charging current for optimum performance. At the low end, currents of less than 1 A are undesirable.
because circuit leakages will contribute significant errors at high temperatures. At higher currents (I > 5mA), transistor betas and saturation voltages will contribute increasingly larger errors. Optimum performance will, therefore, be obtained with charging currents of 10 mA to 1mA. If pins 7 and 8 are shorted together, the magnitude of the charging current due to RA can be calculated from:

\[
l = \frac{R_A}{R_1 + R_2} \cdot \frac{1}{R_2} \cdot \frac{0.2(V_+ - V_-)}{P_A}
\]

R1 and R2 are shown in the Detailed Schematic.
A similar calculation holds for RB.
The capacitor value should be chosen at the upper end of its possible range.

**Waveform Out Level Control and Power Supplies**

The waveform generator can be operated either from a single power supply (10V to 30V) or a dual power supply (±5V to ±15V). With a single power supply the average levels of the triangle and sine wave are at exactly one-half of the supply voltage, while the square wave alternates between V+ and ground. A split power supply has the advantage that all waveforms move symmetrically about ground.

The square wave output is not committed. A load resistor can be connected to a different power supply, as long as the applied voltage remains within the breakdown capability of the waveform generator (30V). In this way, the square wave output can be made TTL compatible (load resistor connected to +5V) while the waveform generator itself is powered from a much higher voltage.

**Frequency Modulation and Sweeping**

The frequency of the waveform generator is a direct function of the DC voltage at Terminal 8 (measured from V+). By altering this voltage, frequency modulation is performed. For small deviations (e.g. ±10%) the modulating signal can be applied directly to pin 8, merely providing DC decoupling with a capacitor as shown in Figure 5A. An external resistor between pins 7 and 8 is not necessary, but it can be used to increase input impedance from about 8kΩ (pins 7 and 8 connected together), to about (R + 8kΩ).

For larger FM deviations or for frequency sweeping, the modulating signal is applied between the positive supply voltage and pin 8 (Figure 5B). In this way the entire bias for the current sources is created by the modulating signal, and a very large (e.g. 1000:1) sweep range is created (f = 0 at VSWEEP = 0). Care must be taken, however, to regulate the supply voltage; in this configuration the charge current is no longer a function of the supply voltage (yet the trigger thresholds still are) and thus the frequency becomes dependent on the supply voltage. The potential on Pin 8 may be swept down from V+ by (1/3 VSUPPLY - 2V).

![FIGURE 5A. CONNECTIONS FOR FREQUENCY MODULATION](image)
Typical Applications

The sine wave output has a relatively high output impedance (1kΩ Typ). The circuit of Figure 6 provides buffering, gain and amplitude adjustment. A simple op amp follower could also be used.

With a dual supply voltage the external capacitor on Pin 10 can be shorted to ground to halt the ICL8038 oscillation. Figure 7 shows a FET switch, diode ANDed with an input strobe signal to allow the output to always start on the same slope.
To obtain a 1000:1 Sweep Range on the ICL8038 the voltage across external resistors RA and RB must decrease to nearly zero. This requires that the highest voltage on control Pin 8 exceed the voltage at the top of RA and RB by a few hundred mV. The Circuit of Figure 8 achieves this by using a diode to lower the effective supply voltage on the ICL8038.

The large resistor on pin 5 helps reduce duty cycle variations with sweep. The linearity of input sweep voltage versus output frequency can be significantly improved by using an op amp as shown in Figure 9.

![Figure 8. VARIABLE AUDIO OSCILLATOR, 20Hz TO 20kHz](image)

![Figure 9. WAVEFORM GENERATOR USED AS STABLE VCO IN A PHASE-LOCKED LOOP](image)
Use in Phase Locked Loops

Its high frequency stability makes the ICL8038 an ideal building block for a phase locked loop as shown in Figure 10. In this application the remaining functional blocks, the phase detector and the amplifier, can be formed by a number of available ICs (e.g., MC4344, NE562, HA2800, HA2820).

In order to match these building blocks to each other, two steps must be taken. First, two different supply voltages are used and the square wave output is returned to the supply of the phase detector. This assures that the VCO input voltage will not exceed the capabilities of the phase detector. If a smaller VCO signal is required, a simple resistive voltage divider is connected between pin 9 of the waveform generator and the VCO input of the phase detector.

Second, the DC output level of the amplifier must be made compatible to the DC level required at the F/M input of the waveform generator (pin 8, 0.8V+). The simplest solution here is to provide a voltage divider to V+ (R1, R2 as shown) if the amplifier has a lower output level, or to ground if its level is higher. The divider can be made part of the low-pass filter.

This application not only provides for a free-running frequency with very low temperature drift, but is also has the unique feature of producing a large reconstituted sinewave signal with a frequency identical to that at the input.

For further information, see Harris Application Note AN013, “Everything You Always Wanted to Know About the ICL8038”.

FIGURE 10. LINEAR VOLTAGE CONTROLLED OSCILLATOR
**Definition of Terms**

Supply Voltage ($V_{\text{SUPPLY}}$). The total supply voltage from $V_+ \text{ to } V_-$. Supply Current. The supply current required from the power supply to operate the device, excluding load currents and the currents through $R_A$ and $R_B$. Frequency Range. The frequency range at which the square wave output through the circuit is guaranteed. Sweep FM Range. The ratio of maximum frequency to minimum frequency which can be obtained by applying a sweep voltage to pin 8. For correct operation, the sweep voltage should be within the range:

$$\frac{2}{3} V_{\text{SUPPLY}} + 2V < V_{\text{Sweep}} < V_{\text{SUPPLY}}$$

FM Linearity. The percentage deviation from the best fit straight line on the control voltage versus output frequency curve.

Output Amplitude. The peak-to-peak signal amplitude appearing at the outputs. Saturation Voltage. The output voltage at the collector of $Q_{23}$ when the transistor is turned on. It is measured for a sink current of 2mA. Rise and Fall Times. The time required for the square wave output to change from 10% to 90%, or 90% to 10%, of its final value. Triangle Waveform Linearity. The percentage deviation from the best fit straight line on the rising and falling triangle waveform.

Total Harmonic Distortion. The total harmonic distortion at the sine wave output.

**Typical Performance Curves**

[FIGURE 11. SUPPLY CURRENT vs SUPPLY VOLTAGE]

[FIGURE 12. FREQUENCY vs SUPPLY VOLTAGE]

[FIGURE 13. FREQUENCY vs TEMPERATURE]

[FIGURE 14. SQUARE WAVE OUTPUT RISE/FALL TIME vs LOAD RESISTANCE]
FIGURE 19. SINE WAVE OUTPUT VOLTAGE vs FREQUENCY

FIGURE 20. SINE WAVE DISTORTION vs FREQUENCY
ICL8038

Introduction

The 8038 is a function generator capable of producing sine, square, triangular, sawtooth and pulse waveforms (some at the same time). Since its introduction, marketing and application engineers have been manning the phones explaining the care and feeding of the 8038 to customers worldwide. This experience has enabled us to form articulate responses to the most frequently asked questions. So, with data sheet and breadboard in hand, read on and be enlightened.

Question 1

I want to sweep the frequency externally but can only get a range of 100:1 (or 50:1, or 10:1). Your data sheet says 1000:1. How much sweep range can I expect?

Answer

Let’s look at what determines the output frequency. Start by examining the circuit schematic at pin 8 in the upper left hand corner. From pin 8 to pin 5 we have the emitter-base of NPN Q1 and the emitter-base of PNP Q2. Since these two diode drops cancel each other (approximately), the potential at pins 8, 5, and 4 are the same. This means that the voltage from V+ to pin 8 is the same as the voltage across external resistors RA and RB. This is a textbook example of a voltage across two resistors which produce two currents to charge and discharge a capacitor between two fixed voltages. This is also a linear system. If the voltage across the resistors is dropped from 10V to 1V, the frequency will drop by 10:1. Changing from 1V to 0.1V will also change the frequency by 10:1. Therefore, by causing the voltage across the external resistors to change from say 10V to 10mV, the frequency can be made to vary at least 1000:1. There are, however, several factors which make this large sweep range less than ideal.

Question 2

You say I can vary the voltage on pin 8 (FM sweep input) to get this large range, yet when I short pin 8 to V+ (pin 6), the ratio is only around 100:1.

Answer

This is often true. With pin 8 shorted to V+, a check on the potentials across the external RA and RB will show 100mV or more. This is due to the VBE mismatch between Q1 and Q2 (also Q1 and Q3) because of the geometries and current levels involved. Therefore, to get smaller voltages across these resistors, pin 8 must be raised above V+.

Question 3

How can I raise pin 8 above V+ without a separate power supply?
**Answer**

First of all, the voltage difference need only be a few hundred millivolts so there is no danger of damaging the 8038. One way to get this higher potential is to lower the supply voltage on the 8038 and external resistors. The simplest way to do this is to include a diode in series with pin 6 and resistors RA and RB. See Figure 1. This technique should increase the sweep range to 1000:1.

![Figure 1. VARIABLE AUDIO OSCILLATOR, 20Hz TO 20kHz](image)

**Question 4**

O.K., now I can get a large frequency range, but I notice that the duty cycle and hence my distortion changes at the lowest frequencies.

**Answer**

This is caused partly by a slight difference in the VBEs of Q2 and Q3. In trying to manufacture two identical transistors, it is not uncommon to get VBE differences of several millivolts or more. In the standard 8038 connection with pins 7 and 8 connected together, there are several volts across RA and RB and this small mismatch is negligible. However, in a swept mode with the voltage at pin 8 near V+ and only tens of millivolts across RA and RB, the VBE mismatch causes a larger mismatch in charging currents, hence the duty cycle changes. For lowest distortion then, it is advisable to keep the minimum voltage across RA and RB around 100mV. This would of course, limit the frequency sweep range to around 100:1.

**Question 5**

I have a similar duty cycle problem when I use high values of RA and RB. What causes this?

**Answer**

There is another error term which becomes important at very low charge and
discharge currents. This error current is the emitter current of Q7. The application note on
the 8038 gives a complete circuit description, but it is sufficient to know that the current
charging the capacitor is the current in RA which flows down through diode Q9 and into
the external C. The discharge current is the current in RB which flows down through diode
Q8. Adding to the Q8 current is the current of Q7 which is only a few microamperes.
Normally, this Q7 current is negligible, but with a small current in RB, this current will
cause a faster discharge than would be expected. This problem will also appear in sweep
circuits when the voltage across the external resistors is small.

Question 6
How can I get the lowest distortion over the largest frequency sweep range.

Answer
First of all, use the largest supply voltage available (15V or +30V is convenient).
This will minimize VBE mismatch problems and allow a wide variation of voltage on pin 8.
The potential on pin 8 may be swept from VCC (and slightly higher) to 2/3 VCC +2V
where VCC is the total voltage across the 8038. Specifically for 15V supplies (+30V),
the voltage across the external resistors can be varied from 0V to nearly 8V before clipping
of the triangle waveform occurs. Second, keep the maximum currents relatively large (1mA
or 2mA) to minimize the error due to Q7. Higher currents could be used, but the small
geometry transistors used in the 8038 could give problems due to VCE(SAT) and bulk
resistance, etc. Third, and this is important, use two separate resistors for RA and RB
rather than one resistor with pins 4 and 5 connected together. This is because transistors
Q2 and Q3 form a differential amplifier whose gain is determined by the impedance
between pins 4 and 5 as well as the quiescent current. There are a number of implications
in the differential amplifier connection (pins 4 and 5 shorted). The most obvious is that the
gain determines the way the currents split between Q2 and Q3. Therefore, any small offset
or differential voltage will cause a marked imbalance in the charge and discharge currents
and hence the duty cycle. A more subtle result of this connection is the effective
capacitance at pin 10. With pins 4 and 5 connected together, the “Miller Effect” as well as
the compound transistor connection of Q3 and Q5 can produce several hundred
picofarads at pin 10, seriously limiting the highest frequency of oscillation. The effective
capacitance would have to be considered important in determining what value of external
C would result in a particular frequency of oscillation. The single resistor connection is fine
for very simple circuits, but where performance is critical, the two separate resistors for RA
and RB are recommended. Finally, trimming the various pins for lowest distortion deserves
some attention. With pins 7 and 8 connected together and the pot at pin 7 and 8 externally
set at its maximum, adjust the ratio of RA and RB for 50% duty cycle. Then adjust a pot on
pin 12 or both pins 1 and 12 depending on minimum distortion desired. After these trims
have been made, set the voltage on pin 8 for the lowest frequency of interest. The principle
error here is due to the excess current of Q7 causing a shift in the duty cycle. This can be
partially compensated for by bleeding a small current away from pin 5. The simplest way to
do this is to connect a high value of resistance (10M to 20M) from pin 5 to V- to bring
the duty cycle back to 50%. This should result in a reasonable compromise between low
distortion and large sweep range.

Question 7
This waveform generator is a piece of junk. The triangle wave is non-linear and has
large glitches when it changes slope.
Answer
You're probably having trouble keeping the constant voltage across RA and RB really constant. The pulse output on pin 9 puts a moderate load on both supplies as it switches current on and off. Changes in the supply reflect as variations in charging current, hence non-linearity. Decoupling both power supply pins to ground right at the device pins is a good idea. Also, pins 7 and 8 are susceptible to picking up switching transients (this is especially true on printed circuit boards where pins 8 and 9 run side by side). Therefore, a capacitor (0.1 F or more) from V+ to pin 8 is often advisable. In the case when the pulse output is not required, leave pin 9 open to be sure of minimizing transients.

Question 8
What is the best supply voltage to use for lowest frequency drift with temperature?

Answer
The 8038AM, 8038AC, 8038BM and 8038BC are all temperature drift tested at VCC = +20V (or 10V). A curve in the lower right hand corner of Page 4 of the data sheet indicates frequency versus temperature at other supply voltages. It is important to connect pins 7 and 8 together.

Question 9
Why does connecting pin 7 to pin 8 give the best temperature performance?

Answer
There is a small temperature drift of the comparator thresholds in the 8038. To compensate for this, the voltage divider at pin 7 uses thin film resistors plus diffused resistors. The different temperature coefficients of these resistors causes the voltage at pins 7 and 8 to vary 0.5mV/oC to maintain overall low frequency drift at VCC = 20V. At higher supply voltages, e.g., 15V (+30V), the threshold drifts are smaller compared with the total supply voltage. In this case, an externally applied constant voltage at pin 8 will give reasonably low frequency drift with temperature.

Question 10
Your data sheet is very confusing about the phase relationship of the various waveforms.

Answer
Sorry about that! The thing to remember is that the triangle and sine wave must be in phase since one is derived from the other. A check on the way the circuit works shows that the pulse waveform on pin 9 will be high as the capacitor charges (positive slope on the triangle wave) and will be low during discharge (negative slope on the triangle wave). The latest data sheet corrects the photograph Figure 7 on Page 5 of the data sheet. The 20% duty cycle square wave was inverted, i.e., should be 80% duty cycle. Also, on that page under “Waveform Timing” the related sentences should read “RA controls the rising portion of the triangle and sine-wave and the 1 state of the square wave.” Also, “the falling portion of the triangle and sine wave and the 0 state of the square wave is:”
**Question 11**
Under Parameter Test Conditions on Page 3 of your 8038 data sheet, the suggested value for Min and Max duty cycle adjust don’t seem to work.

**Answer**
The positive charging current is determined by RA alone since the current from RB is switched off. (See 8038 Application Note AN012 for complete circuit description.) The negative discharge current is the difference between the RA current and twice the RB current. Therefore, changing RB will affect only the discharge time, while changing RA will affect both charge and discharge times. For short negative going pulses (greater than 50% duty cycle) we can lower the value of RB (e.g., RA = 50k and RB = 1.6k). For short positive going pulses (duty cycles less than 50%) the limiting values are reached when the current in RA is twice that in RB (e.g., RB = 50k). This has been corrected on the latest data sheet.

**Question 12**
I need to switch the waveforms off and on. What’s a good way to strobe the 8038?

**Answer**
With a dual supply voltage (e.g., 15V) the external capacitor (pin 10) can be shorted to ground so that the sine wave and triangle wave always begin at a zero crossing point. Random switching has a 50/50 chance of starting on a positive or negative slope. A simple AND gate using pin 9 will allow the strobe to act only on one slope or the other, see Figure 2. Using only a single supply, the capacitor (pin 10) can be switched either to V+ or ground to force the comparator to set in either the charge or discharge mode. The disadvantage of this technique is that the beginning cycle of the next burst will be 30% longer than the normal cycle.

**Question 13**
How can I buffer the sine wave output without loading it down?

**Answer**
The simplest circuit is a simple op amp follower as shown in Figure 3A. Another circuit shown in Figure 3B allows amplitude and offset controls without disturbing the 8038. Either circuit can be DC or AC coupled. For AC coupling the op amp non-inverting input must be returned to ground with a 100k resistor.

**Question 14**
Your 8038 data sheet implies that all waveforms can operate up to 1MHz. Is this true?

**Answer**
Unfortunately, only the square wave output is useful at that frequency. As can be seen from the curves on page 4 of the data sheet, distortion on the sine wave and linearity
of the triangle wave fall off rapidly above 200kHz.

**Question 15**

Is it normal for this device to run hot to the touch?

**Answer**

Yes. The 8038 is essentially resistive. The power dissipation is then E^2/R and at 15V, the device does run hot. Extensive life testing under this operating condition and maximum ambient temperature has verified the reliability of this product.

**Question 16**

How stable are the output amplitudes versus temperature?

**Answer**

The amplitude of the triangle waveform decreases slightly with temperature. The typical amplitude coefficient is -0.01%/°C, giving a drop of about 1% at 125°C. The sine output is less sensitive and decreases only about 0.6% at 125°C. For the square wave output the VCE(SAT) goes from 0.12V at 25°C to 0.17V at 125°C. Leakage current in the “1” state is less than a few nanoamperes even at 125°C and is usually negligible.
Schematic Diagram
MEGGITT CGS

HIGH VOLTAGE RESISTORS
HIGH VALUE RESISTORS
HIGH POWER RESISTORS
ALUMINIUM CLAD RESISTORS
CURRENT SENSE RESISTORS

High Value Resistors
TYPE HBS SERIES

The HBS is a high voltage plate resistor offering resistance values up to 1 Teraohm and working voltages up to 30 KV. A tough lacquer coating encapsulates the product so that excellent TCR's and VCR's are maintained. This is a sister product to the HBO Series, effectively extending the value range that is available. Further options are also available with the ability to produce custom designs relatively quickly where quantities justify.

MEGGITT CGS KEY FEATURES

- ELEMENT VOLTAGE UPTO 30KV
- EXCELLENT TO SIZE POWER RATIO
- HIGH RELIABILITY
- LOW NOISE AT LOW VALUES
- RESISTANCE VALUES UPTO 1 TERA OHM
- NON INDUCTIVE
- CUSTOM DESIGNS PARTICULARLY WELCOME
SPECIFICATION TYPE HBS SERIES

ELECTRICAL

<table>
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<th>Working Voltage</th>
<th>Watts at 70°C</th>
<th>Range</th>
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<td>1.0</td>
<td>1.0</td>
<td>1 Meg - 1 Terahertz</td>
</tr>
<tr>
<td>HBS40</td>
<td>29.0</td>
<td>1.2</td>
<td>1 Meg - 1 Terahertz</td>
</tr>
<tr>
<td>HBS50</td>
<td>30.0</td>
<td>3.0</td>
<td>1 Meg - 1 Terahertz</td>
</tr>
</tbody>
</table>

Resistance Tolerance:
1%, 2%, 5%, 10%, 20%, 30%

Temperature Coefficient:
-1M to 99.9M: ±60, 100, 250 ppm/°C
-99M to 500M: ±50, 100, 250 ppm/°C
-500M to 1T: ±250, 500, 1000 ppm/°C

Voltage Coefficient:
1M to 99.9M: <2ppm/V
99M to 500M: <100ppm/V
500M to 1T: <500ppm/V
1T: <1000ppm/V

N.B. Measuring Voltage of 10KV is used.

ENVIRONMENTAL

Ambient Temperature Range: T.C.R. >100ppm/°C - 55°C to +125°C
TC.R. <100ppm/°C - +25°C to +125°C

Chromatic Category: 55/125/56

LONG TERM STABILITY

Storage 125°C/1000 hrs <10 Gtg.
Less than 1%

Storage 125°C/1000 hrs >10 Gtg.
Less than 1%

Maximum Voltage/1000 hrs <10 Gtg.
Less than 1%

Maximum Voltage/1000 hrs >10 Gtg.
Less than 2%

Encapsulation: Lacquer Coating

DIMENSIONS

![Diagram of dimensions]

PACKAGING

Plastic bagged tubes

MINIMUM ORDER QTY:
100 Pieces per tube

HOW TO ORDER

<table>
<thead>
<tr>
<th>Model</th>
<th>Name/Description</th>
<th>Resistance Value</th>
<th>Tolerance</th>
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<tbody>
<tr>
<td>HBS</td>
<td></td>
<td></td>
<td>F = ±1%</td>
</tr>
</tbody>
</table>

All Dimensions are in millimeters

Din DIN Scale

1. L1 = 8.5
2. L2 = 12.5
3. H1 = 3.3
4. D = 6.3